CLAIMS

1. Method for improving the reliability of a computer system, said system comprising:

a bus (PCI);

an interface circuit (1); and

a plug-in unit (2), which is connected to the bus via the interface circuit (1); and

in which method the plug-in unit (2) is addressed via the bus (PCI), characterized in that:

addressing operations directed at the plug-in unit (2) are monitored by the interface circuit;

the duration of addressing of the plug-in unit is measured; and when the duration exceeds a predetermined period of time, then

the addressing is terminated.

2. Method as defined in claim 1, characterized in that the duration of addressing is monitored using a watchdog timer (3) with a predetermined timing set in it.

3. Method as defined in claim 1 or 2, characterized in that addressing is terminated by sending into the bus (PCI) a signal indicating termination of addressing.

4. Method as defined in claim 1, characterized in that, when addressing has been terminated, an error signal is set by the interface circuit (1) into active state in the bus (PCI).

5. Method as defined in claim 1, characterized in that, when addressing has been terminated, a signal indicating an error condition in the plug-in unit (2) is set by the interface circuit (1) into active state in the status register (STATUS) of the plug-in unit.

6. Interface circuit for improving the reliability of a computer system, said system comprising:

a bus (PCI);

a plug-in unit (2) which is connected to the bus (PCI) via the interface circuit (1);

characterized in that the interface circuit (1) comprises:

a watchdog timer (3);

means (4) for starting the watchdog timer upon the start of addressing; and

means (5) for terminating the addressing.

7. Interface circuit as defined in claim 5, characterized in that the interface circuit (1) comprises means (5) for sending into the bus (PCI) a signal indicating termination of addressing.

8. Interface circuit as defined in claim 5 or 6, characterized in that the interface circuit (1) comprises means (6) for setting an error signal into active state in the bus (PCI).

9. Method as defined in any one of claims 6 - 8, characterized in that the interface circuit (1) comprises means (7) for setting a signal indicating an error condition in the plug-in unit (2) into active state in the status register (STATUS) of the plug-in unit.

10. Interface circuit as defined in claim 6, characterized in that the bus (PCI) is a CompactPCI bus.